

ABSTRACT OF THE DISCLOSURE

An electronic system (1) including an instruction-programmable processor, such as a digital signal processor (2), having a level one program cache memory and instruction buffer subsystem (38), is disclosed. The level one program cache memory and instruction buffer subsystem (38) includes a program data random access memory (RAM) (60), in combination with a tag RAM (54) and a tag comparator (58), and a loop cache subsystem (62, 62') in parallel with the program data RAM (60). An instruction fetch unit (10) presents fetch addresses to the tag comparator (58) and to the loop cache subsystem (62; 62'). The loop cache subsystem (62, 62') includes a branch cache register file (76; 176) for storing instruction opcodes corresponding to a sequence of fetch addresses beginning with a base address. If the fetch address issued by the instruction fetch unit (10) is a hit relative to the loop cache subsystem (62; 62'), loop cache control logic (74; 174) disables reads from the program data RAM (60) in favor of accesses to the branch cache register file (76; 176). According to one disclosed embodiment, the branch cache register file (76) is loaded with opcodes beginning with each backward branch that is a miss relative to the branch cache register file (76). According to another disclosed embodiment, the branch cache register file (176) is loaded with opcodes beginning with backward branches that are a miss relative to the branch cache register file (176) and that have been executed twice in succession.

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